Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.089”**

**.075”**

**CATHODE**

**Top Material: Au**

**Backside Material: Au**

**Bond Pad Size: .067” X .075”**

**Backside Potential: ANODE?**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .078” X .089” DATE: 9/2/21**

**MFG: MICROSEMI THICKNESS .009” P/N: 1N5811**

**DG 10.1.2**

#### Rev B, 7/1